	Ministry of Higher Education and Scientific Research - Iraq University of Warithe Al_Anbiyaa Engineering College Biomedical Engineering Department	

MODULE DESCRIPTION FORM

Module Information					
Module Title	Electronic Circuits II			**Module Delivery**	
Module Type	Basic			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	BME-211				
ECTS Credits	7				
SWL (hr/sem)	175				
Module Level			**Semester of Delivery**	1	
Administering Department	BME		**College**	ENG	
Module Leader	Ali mohammed abdulsadaa		**e-mail**	Ali.mohammed@uowa.edu.iq	
Module Leader's Acad. Title	Assistant lecture		**Module Leader's Qualification**	Ph.D.	
Module Tutor			**e-mail**		
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date	2026/2/20		**Version Number**	1.0	

Relation with other Modules			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents	
Module Aims	1. Develop problem-solving skills and an understanding of electronic circuits through practical application. 2. Understand the analysis and application of diode circuits. 3. Understand scissor, clamp, and Zener circuits. 4. This course covers the fundamental concepts of electronic circuits. 5. Understand and analyze the main types of transistors. 6. Perform series-connection analysis of transistors.
Module Learning Outcomes	1. An ability to identify, formulate, and solve engineering problems by applying principles of engineering, science, and mathematics. 2. An ability to apply engineering design process to produce solutions that meet specified needs with consideration of public health, safety, and global, cultural, social, environmental, economic, and other factors as appropriate to the discipline. 3. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw a conclusion.
Indicative Contents	Indicative content includes the following. Semiconductors: N-type, P-type, P-N junction, V-I characteristics, diode applications, half-wave rectifier, full-wave rectifier, power supply with filters and regulators, clippers, clamps, Zener diode: construction, characteristics and circuitry, applications, other types of diodes: variable diodes, current-regulating diode, tunneling diode, shock diode, PIN diode, bipolar junction transistor (BJT): transistor structure, BJT connection configuration, bias, characteristics, amplification parameters, DC load line, waveform distortion and Q-point, BJT switching operation, BJT amplifier operation, H parameters, equivalent circuits for CC, CB, and C.E. with their circuit applications.

Learning and Teaching Strategies	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL)			
Structured SWL (h/sem)	93	**Structured SWL (h/w)**	6
Unstructured SWL (h/sem)	57	**Unstructured SWL (h/w)**	4
Total SWL (h/sem)	150		

Module Evaluation					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	**Midterm Exam**	3 hrs.	10% (10)	7	LO # 1-7
	Final Exam	3 hrs.	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)	
	Material Covered
Week 1	Semiconductors: N-type, P-type, P-N junction, V-I characteristics
Week 2	Diode applications, half-wave rectifier, full-wave rectifier
Week 3	Parameters, DC load line, Q-point and waveform distortion
Week 4	Power supplies with filters and regulators, clippers, clampers
Week 5	Zener diode: construction, characteristics, circuitry and applications
Week 6	Bipolar junction transistor (BJT): transistor structure
Week 7	Midterm exam
Week 8	BJT connection configuration, bias, characteristics, and amplification
Week 9	BJT switching operation
Week 10	BJT amplifier operation
Week 11	H parameters, equivalent circuits
Week 12	H parameters, equivalent circuits for C.C.
Week 13	H parameters, equivalent circuits for C.B.
Week 14	H parameters, equivalent circuits for CE with their circuit applications
Week 15	Darlington amplifier
Week 16	Preparation week before the final exam

Delivery Plan (Weekly Lab. Syllabus)	
	Material Covered
Week 1	Diode characteristics
Week 2	Types of diode
Week 3	Rectifiers and filters
Week 4	Clippers, clippers, and voltage amplifiers
Week 5	Zener diode as a voltage regulator
Week 6	BJT characteristics and DC bias
Week 7	Common-emitter amplifier

Learning and Teaching Resources		
	Text	**Available in the Library?**
Required Texts	Boylestad, R.L., and Nashelsky, L., Electronic Devices and circuit Theory, 9th Ed., Pearson Education, Inc., 2013.	Yes
Recommended Texts	Floyd, Thomas L., Electronic devices: Electron Flow Version, 11th Ed., Pearson Education, Inc., 2012.	No
Websites	https://www.coursera.org/browse/physical-science-and-engineering/electrical-engineering	

Grading Scheme			
Group	**Grade**	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A -** Excellent	90 - 100	Outstanding Performance
	B - Very Good	80 - 89	Above average with some errors
	C - Good	70 - 79	Sound work with notable errors
	D - Satisfactory	60 - 69	Fair but with major shortcomings
	E - Sufficient	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	(45-49)	More work required but credit awarded
	F – Fail	(0-44)	Considerable amount of work required
Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.			